Sheet: Gate & Skip

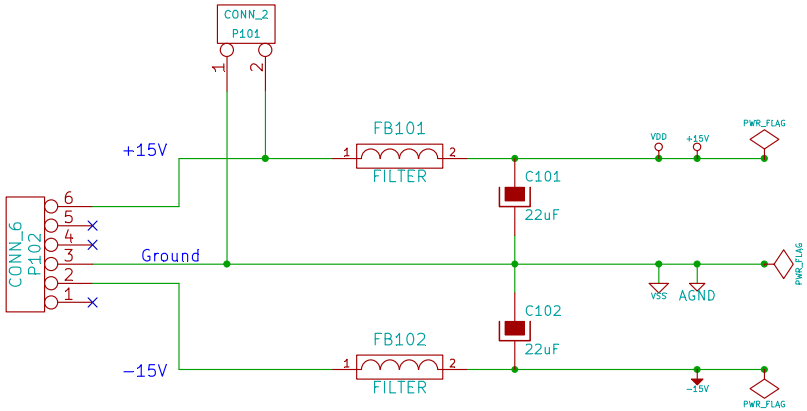
File: Gate & Skip bus V2.sch

Sheet: CVA

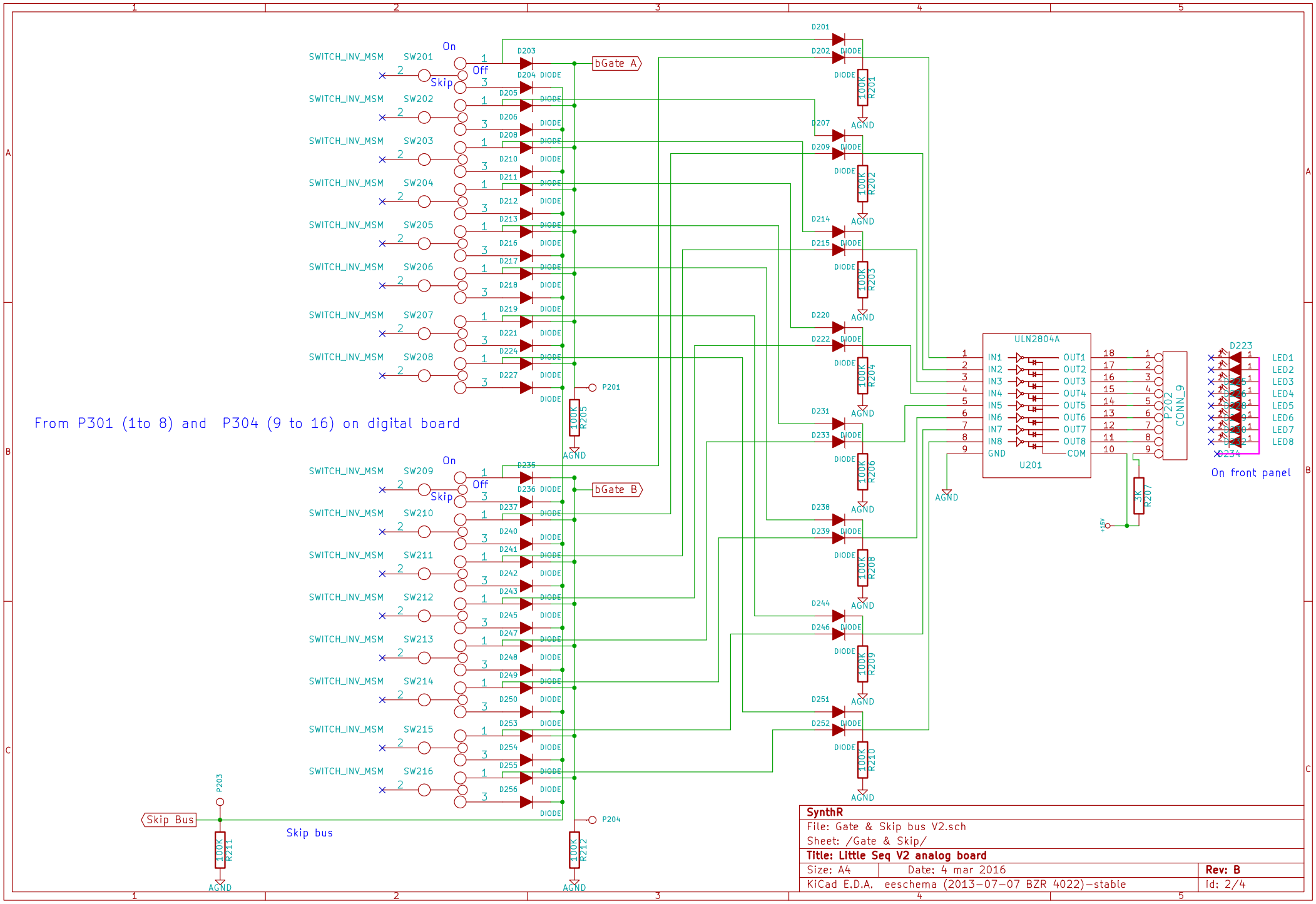
File: CvA V2.sch

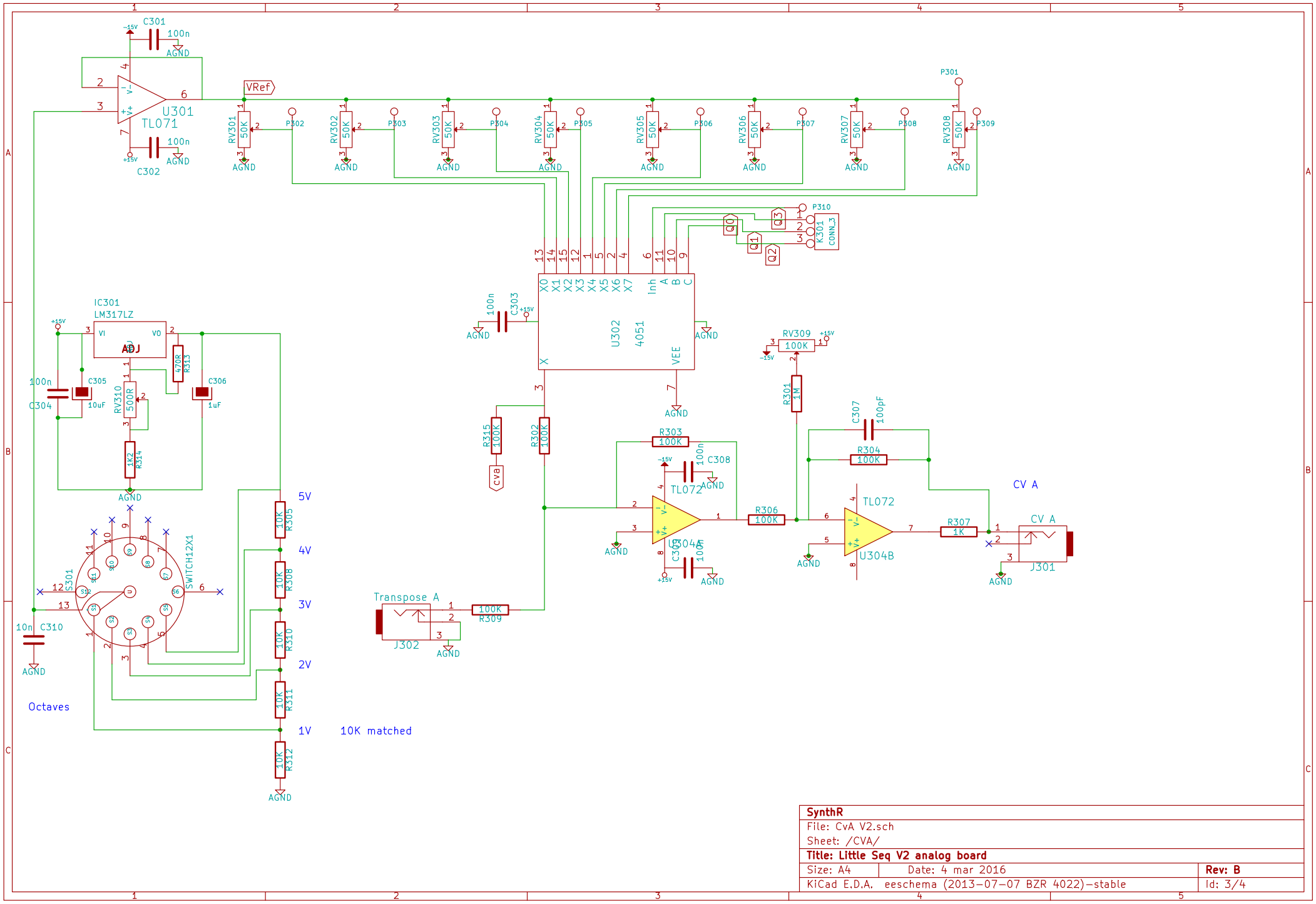
Sheet: CVB

File: CvB V2.sch

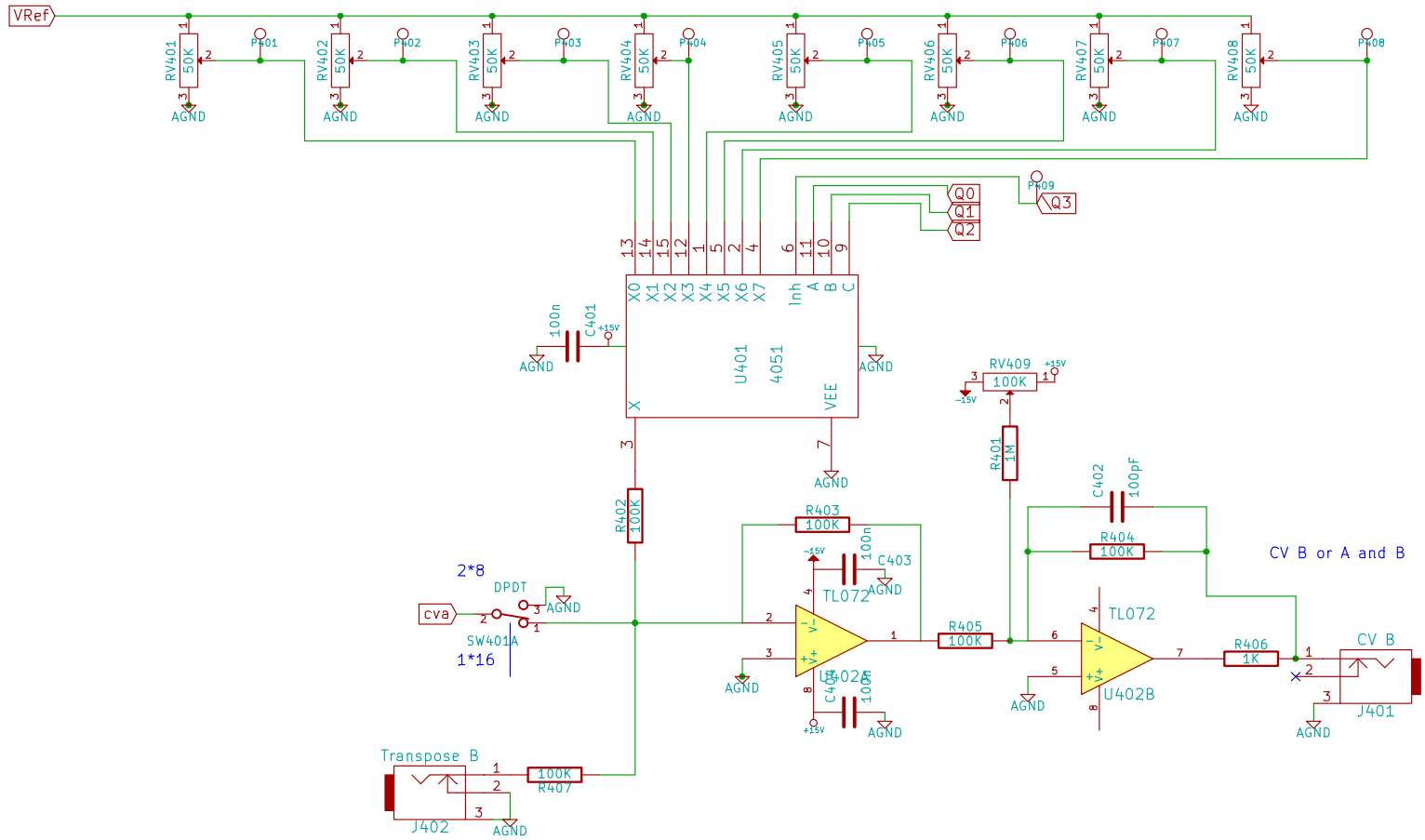


SynthR		
File: Little Seq V2 analog.sch		
Sheet: /		
Title: Little Seq V2 analog board		
Size: A4	Date: 4 mar 2016	**Rev: B**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 1/4


From P301 (1to 8) and P304 (9 to 16) on digital board
SWITCH_INV_MSM
SW201
SW202
SW203
SW204
SW205
SW206
SW207
SW208
SW209
SW210
SW211
SW212
SW213
SW214
SW215
SW216
On
Off
Skip
bGate A
bGate B
DIODE
100K
AGND
P201
P202
P203
P204
Skip Bus
Skip bus
ULN2804A
U201
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
GND
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
COM
CONN_9
3K
R207
+15V
D223
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
On front panel
SynthR
File: Gate & Skip bus V2.sch
Sheet: /Gate & Skip/
Title: Little Seq V2 analog board
Size: A4
Date: 4 mar 2016
Rev: B
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 2/4



SynthR		
File: CvA V2.sch		
Sheet: /CVA/		
Title: Little Seq V2 analog board		
Size: A4	Date: 4 mar 2016	**Rev: B**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 3/4



SynthR		
File: CvB V2.sch		
Sheet: /CVB/		
Title: Little Seq V2 analog board		
Size: A4	Date: 4 mar 2016	**Rev: B**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 4/4